

**Notice of Allowability**

Application No.

10/727,647

Examiner

Andy Huynh

Applicant(s)

TAKEUCHI ET AL.

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**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the Pre-Amendment dated 02/02/2004.
2. ☒ The allowed claim(s) is/are 47-74.
3. ☒ The drawings filed on 05 December 2003 are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☒ All    b) ☐ Some\*    c) ☐ None    of the:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☒ Certified copies of the priority documents have been received in Application No. 10/098,130.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
  6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
    - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
    - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08),  
Paper No./Mail Date 12/05/03
4. ☐ Examiner's Comment Regarding Requirement for Deposit  
of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413),  
Paper No./Mail Date \_\_\_\_\_.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_.

  
David Nelms

Supervisory Patent Examiner  
Technology Center 2800

### **DETAILED ACTION**

In the Preliminary Amendment dated February 02, 2003, Applicant has canceled claims 1-46, amended claims 47-48 and added new claims 49-74 is acknowledged. Accordingly, claims 47-74 are pending in the application, which is a divisional of application Serial No. 10/098,130 filed 03/15/2002, USP 6,720,612 dated 04/13/2004.

#### ***Allowable Subject Matter***

Claims 47-74 are allowed.

The following is an examiner's statement of reason for allowance: The prior art of record fails to teach or suggest the limitation recited a method of manufacturing a semiconductor device comprising: forming a first insulating film not containing nitrogen as a major component on said semiconductor substrate to cover said first gate electrode and said second gate electrode in such a manner that a portion of said first insulating film is embedded between said first gate electrode and said second gate electrode to a height above a height of said first gate electrode; forming a second insulating film on said first insulating film; forming on said second insulating film an interlayer insulating film whose etching rate is larger than an etching rate of said second insulating film as claimed in independent claim 47; a method of manufacturing a semiconductor device comprising: forming a first insulating film not containing nitrogen as a major component on said semiconductor substrate to cover said first memory cell gates, said second memory cell gates and said diffusion layers in such a manner that portions of said first insulating film are embedded between said first memory cell gates or between said second memory cell gates, a

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portion of said first insulating film is provided on one of said diffusion layers, on which one of said pair of first selecting gates is adjacent to one of said pair of second selecting gates in such a manner that a part of said portion of said first insulating film, which is on a major part of said one of said diffusion layers, has a thickness thinner than a thickness of said portions of said first insulating film, which are embedded between said first memory cell gates and between said second memory cell gates; forming a second insulating film on said first insulating film; forming on said second insulating film an interlayer insulating film whose etching rate is larger than an etching rate of said second insulating film as claimed in independent claim 48; and a method of manufacturing a semiconductor device comprising: forming a first insulating film not containing nitrogen as a major component on said semiconductor substrate to cover said first gate electrode and said second gate electrode in such a manner that a portion of said first insulating film is embedded between said first gate electrode and said second gate electrode to a height above a height of said first gate electrode, another portion of said first insulating film is provided on a major part of said first or second diffusion layer to a height lower than a height of said first gate electrode; forming a second insulating film on said first insulating film; forming on said second insulating film an interlayer insulating film whose etching rate is larger than an etching rate of said second insulating film as claimed in independent claim 73.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

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***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh whose telephone number is (571) 272-1781. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



AH

04/28/04



David Nelms  
Supervisory Patent Examiner  
Technology Center 2800